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SEMICONDUCTOR INTEGRATED CIRCUIT

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[There are no amendments to this patent.]

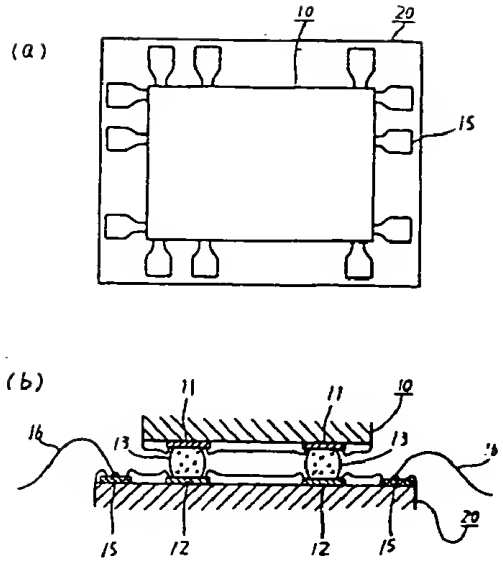
Abstract

Objective

It relates to a semiconductor integrated circuit provided with memory cells, and the objective is to improve the integration without increasing the area occupied by the chip, increase the line width of the internal wiring, and enhance the freedom in the layout.

Constitution

The necessary semiconductor integrated circuit is formed by forming circuit blocks with mutually different functions on separate chips like the memory cells and the peripheral circuits, superimposing these chips, then mutually connecting these. As a result, formation of internal wiring of high reliability and low resistance becomes possible.



Explanatory figure for Application Example 1 of the present invention.

Claims

1. A semiconductor integrated circuit characterized by the fact that it was provided with a first chip which is formed with a first semiconductor integrated circuit and has a surface exposed with a plurality of electrodes connected to the input/output terminal of the first semiconductor integrated circuit,

a second chip which is a chip formed with the second semiconductor integrated circuit and has a smaller area than said first chip, has a surface exposed with a plurality of electrodes arranged in a planar symmetrical relationship with said plurality of electrodes in said first chip surface and connected to the input/output terminal of said second semiconductor integrated circuit, and moreover, is arranged on said first chip so that said surface opposes the surface of said first chip, and

a connecting means for mutually connecting said plurality of electrodes in said first chip surface and said plurality of electrodes in said second chip surface.

2. A semiconductor integrated circuit noted in Claim 1, characterized by the fact that it is provided with an electrode which is connected to the input/output terminal of said second semiconductor integrated circuit via said connecting means or the input/output terminal of said first semiconductor integrated circuit at the peripheral area of said first chip, and is connectable with respect to an external circuit.

3. A semiconductor integrated circuit noted in Claim 1 or 2, characterized by the fact that a plurality of said second chips is arranged on said first chip surface.

4. A semiconductor integrated circuit noted in Claims 1, 2, or 3, characterized by the fact that said second integrated circuit includes a memory cell and said first integrated circuit includes a peripheral circuit for driving said memory cell.

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